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Space weather Observations at Lagrange 1 to Advance Readiness (SOLAR) Radiation Hardness Assurance Requirements Document (RHARD)

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Space weather Observations at Lagrange 1 to Advance Readiness (SOLAR) Project Radiation Hardness Assurance Requirements Document (RHARD) Review/Signature/Approval Page

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Preface

This document is under Space weather Observations at Lagrange 1 to Advance Readiness (SOLAR) Project configuration control. Once this document is approved, SOLAR approved changes are handled in accordance with Class I and Class II change control requirements as described in the SOLAR Configuration Management Procedure, and changes to this document shall be made by complete revision.

In this plan, all mandatory actions (i.e., requirements) are denoted by statements containing the term “shall.” The terms “may” or “can” denote discretionary privilege or permission; “should” denotes a good practice and is recommended but not required; “will” denotes expected outcome; and “are/is” denotes descriptive material.

Any questions should be addressed to:

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Section # / Rqmt.	Deviation / Waiver #	CCR #	Date Approved	Description
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1 INTRODUCTION

1.1 Scope and Intent

The Generic Class C Radiation Hardness Assurance Requirement Document (RHARD) establishes radiation requirements necessary for systems with Electrical, Electronic, Electromechanical, and Electro-optical (EEEE) parts to implement the project's radiation requirements from the Spacecraft Requirements Document (SRD) and the instruments. This document also outlines the project's plan to control the effects of ionizing and non-ionizing radiation on EEEE parts and systems and provides context for the proper interpretation, implementation, and expected verification of the requirements herein.

1.2 Mission Applicable Documentation

- Spacecraft Requirements Document (SRD), document number SOLAR-SC-REQ-0005, defines the spacecraft requirements including environments applicable to the mission and strategic operational/survivability requirements for each as appropriate for the specific mission.
- Mission Assurance Requirements (MAR), document number SOLAR-SMA-REQ-0006, establishes EEEE Parts Control Plan (PCP) and defines the specific deliverable items to meet mission assurance requirements for payloads of a given risk classification.
- Military Standard (MIL-STD)-750, Test Method 1019
- MIL-STD-705, Test Method 1080
- This test method standard is established for silicon planar-gate vertical MOSFETs and does not address necessary specifics for other device structures or materials.
- MIL-STD-883, Test Method 1019
- Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association, JEDEC Standard JESD57A, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation", November 2017.
- This document does not necessarily address all specifics required to evaluate certain technologies that have not migrated from state of the art to state of the practice.
- ASTM F1192, Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices
- ASTM F1892, Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices

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- NASA Alert NA-GSFC-2005-05

1.3 Interpreting Requirements

Mission radiation requirements are often derived from simple geometric assumptions, bounded environment conditions, and commonly accepted energy deposition thresholds. Detailed analysis of EEEE part radiation response, transport analyses of spacecraft structure, and sophisticated environment assessments are part of a robust radiation hardness assurance program. The project radiation engineer, in consultation with the parts control board, systems engineers, project management, and other stakeholders, is responsible for interpreting and applying these analyses when used to verify radiation requirements. In many circumstances a verification by test or analysis is more complex than meeting one pre-defined value; the project radiation engineer is expected to determine if the intent of the radiation requirements is satisfied by the entirety of available data.

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2 SPACE ENVIRONMENT RADIATION EFFECTS IN EEEE SYSTEMS

The SOLAR mission radiation environment will consist of galactic cosmic ray ions; protons and electrons trapped in the Van Allen belts; protons and heavier ions from solar events; and solar wind plasma consisting of low energy electrons, protons, and heavier ions as described in the SRD. EEEE parts as well as some materials are subject to degradation or anomalous behavior in this environment due to multiple phenomena: Total Ionizing Dose (TID), Displacement Damage Dose (DDD), and both destructive and non-destructive single event effects (SEE).

2.1 Radiation Hardness Assurance Plan

This section provides descriptive context to understand the overall expectations of the SOLAR radiation engineers when designing, developing, or reviewing SOLAR flight hardware. A shorter list of formal requirements follows.

2.1.1 TID/DDD Hardness Assurance Plan

For a Class C mission, the TID/DDD hardness assurance effort focuses on degradation mechanisms that propagate to the system level and affect mission performance prior to end of life. This assessment considers system architecture, circuit design, physical/mechanical spacecraft design, and, ultimately, EEEE parts response to TID/DDD. A combination of generic (non-lot specific) parts test data, flight lot parts test data, architectural design analyses, assessments of likelihood and criticality, and past experience with known technologies/materials is sufficient in most cases to demonstrate a Class C level of risk acceptance. TID/DDD requirements are written for the system level and verification methods are largely left to the implementor.

2.1.1.1 Piece Part Testing Strategy

Across-the-board flight-lot parts testing is neither required nor sufficient on its own for mission success. However, part-level response remains a common means to identify and classify risks. Where EEEE part-level response is critical to system operations, the expectation is at least a 90% confidence that 99% of the flight lot (99/90) shall survive a 95th percentile environment. This is satisfied through either a radiation assessment of existing part/technology data or project radiation testing of the flight lot in accordance with MIL-STD-883 Test Method 1019, MIL-STD-883 Test Method 1017, ESCC Basic Specification No. 22900, or as otherwise prescribed by the project radiation engineer.

2.1.1.2 Use of Specific TID/DDD Levels

Radiation analyses of part or system response are commonly evaluated with the TID/DDD value within a 100 mil Al sphere, or a location-specific value determined by sophisticated radiation transport analysis, when available. 100 mil Al presents a conservative (low) estimate of the shielding presented by most spacecraft and is generally consistent with historical industry/NASA

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parts acceptance processes. However, more sophisticated approaches exist, e.g., radiation transport analysis, that better approximate the real shielding profile at the part or circuit level when necessary or desirable. These sophisticated approaches should be used with caution, as they reduce the levels of conservatism in the analysis. Multiple levels of environmental shielding analysis cannot be calculated independently and then applied together. It has been observed in the past that combining independent vendor-provided radiation shielding analyses and NASA spacecraft-level radiation shielding analyses may underestimate the dose received by a part with spot shielding, particularly for parts sold with integrated spot shielding.

2.1.1.3 Applicability of TID/DDD Test Data

EEEE parts may present non-negligible radiation degradation in one application but not another. All parts are evaluated for each unique application system, and previous approval does not inherently extend to all usage within a project, i.e., parts are not "qualified" for blanket use on a given project. It is further recommended that degradation of individual EEEE parts due to TID/DDD be considered in circuit-level worst-case analyses to demonstrate system tolerance to expected dose levels.

Some EEEE parts present additional nuances when considering acceptable levels of dose and degradation. Parts should always be considered in the context of their fundamental technology and the potential differences between ground-based testing and flight environment recognized. As an example, bipolar and BiCMOS components must consider dose rate effects, e.g., enhanced low dose rate sensitivity (ELDRS) in any analysis or testing. Significant design margin may reduce the risk of ELDRS but cannot entirely eliminate it in certain edge cases.

DDD levels are commonly expressed in units of megaelectronvolts (MeV)/g, in equivalent proton fluence, or 1 MeV neutron equivalent fluence. These are material dependent and many of the parts most susceptible to DDD are not Si based. Conversion between units of DDD is a subject of ongoing study and multiple approaches exist.

The level of accuracy to which flight part degradation (and thus, to some degree, system response) can be predicted is related to the data made available for analysis. Test data at an appropriate dose rate taken from the flight lot is most predictive of flight response; data taken from generic lots, from similar parts, or based on heritage use provide lower levels of predictive value.

In many cases detailed flight-lot test data is not necessary to prove that a part or system is tolerant to TID or DDD. PN junction diodes, bipolar transistors used as low-gain switches in benign orbits, and GaAs MMICs are common examples of parts that may not present credible risk of TID degradation, and most complementary metal–oxide–semiconductor (CMOS) microcircuits have high tolerance to DDD. However, if radiation test, qualification, or characterization data are presented as necessary evidence to verify radiation requirements, the data are expected to be representative of the part and/or system under evaluation, to include an appropriate source and/or dose rate.

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2.1.2 SEE Hardness Assurance Plan

SEE hardness assurance takes different approaches for destructive and non-destructive SEE. Destructive SEE, such as single-event latchup (SEL), single-event gate rupture(SEGR), and single-event burnout (SEB) present a random chance of part-level functional failure when parts are operated in a radiation environment, though failures may not always be immediately catastrophic. Non-destructive SEE, such as single-event upset (SEU), single-event transient (SET), and single-event functional interrupts (SEFI) may interrupt or degrade system performance but are correctable or recoverable. Non-destructive SEE are the most circuit- and application-dependent radiation effects and are often unavoidable in modern EEEE parts, whether radiation-hardened or not.

For a Class C mission, RHA effort focuses on elimination of destructive SEE risk and identification of parts and circuits presenting credible risk of non-destructive single event responses that propagate to the system level. A combination of applicable part test data, past experience with known technologies/materials, and an assessment of the circuit design and system architecture is sufficient in most cases to demonstrate a Class C level of risk acceptance. In limited circumstances flight lot test data is required, particularly for destructive SEE, where circuit-level mitigations and generic part data are less suitable.

2.1.2.1 Piece Part Testing Strategy

Hardness assurance against destructive SEE usually begins at the part level, seeking to identify parts designed to be, or by nature of their technology, insensitive to destructive SEE. While destructive SEE in many cases may be mitigated by electrical derating (particularly for SEB and SEGR) or by circuit design (SEL), each of these phenomena is capable of permanently damaging a part regardless of circuit design. Further, testing at the card or assembly level for destructive SEE is particularly challenging or impossible at most test facilities. Developing a system tolerant to or hardened against destructive SEE is most effectively performed first at the parts level, and then by robust circuit designs when necessary. For these reasons, the Class C RHARD includes requirements for piece-part destructive SEE hardness.

Hardness assurance against non-destructive SEE is the opposite. Here, part performance alone provides little context to the performance of a larger system. Well-characterized parts provide the most thorough information necessary to effectively develop radiation-tolerant circuits and systems, but in many cases, it is possible or even necessary to design for mitigation up front. System tolerance and/or mitigation takes the form of fault isolation, detection, and recovery; error-detection and correction codes (EDACs); filtering circuitry; power-cycling; current limiting; and other techniques to mitigate or eliminate any effect on broader system operation. Verification by testing at the board level is possible, though not universal.

2.1.2.2 Viability of Shielding

While shielding is a common mitigation against total ionizing dose or displacement damage dose, it has limited effectiveness as a mitigation for single-event effects, which can be induced by deeply-penetrating, high-energy particles, e.g., Galactic Cosmic Rays. Shielding analyses are

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welcomed as part of a comprehensive SEE mitigation strategy but are rarely the primary means of SEE tolerance.

2.1.2.3 Applicability of Known Test Data

SEE response is largely dependent on part design and architecture, rather than lot-to-lot process variability. Part data is generally applicable ("flight lot applicable") where there have been no changes to the semiconductor manufacturer mask set, foundry, or process. Parts must also be operated in a manner bounding the conditions used in flight; this includes parameters like voltage, data rate, load current, duty cycle, and so forth. Circuit or system data is applicable only where the design is similar enough that individual part response would reasonably produce the same results at the higher level, e.g., same capacitance on output nodes, same data rate, etc.

Destructive SEEs carry specific additional considerations when evaluating data. It is vital that SEB and SEGR test data be collected in an appropriate manner for their technology; there are large bodies of published test data on radiation-hardened vertical power MOSFETs that do not have the particle range necessary to demonstrate hardness to SEGR. The simple verification of LET requirements provided in this document is not always sufficient, and the underlying data must be checked for correctness.

2.1.2.4 Proper Use of LET Thresholds

Linear Energy Transfer (LET) and LET Thresholds (LET_{th}) are commonly used to describe a part's sensitivity to SEE phenomena. In general, higher LET particles are less common in a space environment and an appropriate LET_{th} determines the types of testing or test data required. However, any threshold LET alone does not imply immunity and a broader analysis of part response, system architecture and operating conditions are necessary to determine if requirements are met. Supporting data to address each part's application, e.g., bias voltage, frequency, etc., is critical to verify these requirements.

Notes on LET:

- LET is dependent upon incoming particle energy, atomic number, and target materials. The amount of charge deposited into a sensitive volume, e.g., transistor, is further dependent upon the path-length and track structure through the target.
- The natural space environment has a precipitous decline in particle populations that exhibit LET greater than 37 $MeV \cdot cm^2/mg$.
- Ion strikes following worst case paths through sensitive volumes may have much higher effective LET. A particle with an LET of 37 $MeV \cdot cm^2/mg$ could deposit as much charge as a particle having LET of 75 $MeV \cdot cm^2/mg$ or more.
- Generally, a LET_{th} of 75 $MeV \cdot cm^2/mg$ or greater is considered to be immune; however, particles of extremely high LET are non-zero.

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- Proton-induced secondaries in silicon and SiC materials have LET less than 20 MeV·cm^2/mg. This range includes the vast majority of fluence for a typical mission.
- There is no arbitrary LET_{th} imposed for devices that show non-destructive SEE. However, devices with LET_{th} greater than 20 MeV·cm^2/mg are recommended to reduce system risks.
- GaN and GaAs materials experience higher LETs than silicon and SiC materials, which should be considered where applicable.

2.1.2.5 SEE Criticality Assessments

System responses to SEE in this document are classified based on function and criticality as follows:

Functional Criticality Classes:

- *Error-Functional* - function may be unaffected by SEE (possibly by error-correction scheme, mitigation, or redundancy); frequent events may be acceptable.
- *Error-Vulnerable* - function where low probability for SEE is required; response by mitigation or characterization and acceptance of risk is permissible.
- *Error-Critical* - function where SEE is unacceptable; part technology, design, or usage must eliminate any probability of error to a specified degree.

Criticality can be assigned as *Error-Functional* for single events that do not propagate to a meaningful level and should not require rate calculation. Examples include analog transients that are filtered by the downstream circuitry, momentary corruption of non-critical or over-sampled engineering telemetry, or single word science loss.

Propagating single event effects may be defined as *Error-Vulnerable* or *Error-Critical*. Vulnerable single event effects are those that are handled locally by mitigation approaches such as EDAC, programmed FPGA memory scrub, etc. Critical single event effects are typically those that require ground intervention or maintenance to correct, i.e., significant loss of functionality).

An evaluation should be conducted to ensure that the mitigation techniques for *Error-Vulnerable* single-event effects are sufficient to keep them from becoming *Error-Critical*. That is, the rate of mitigation should be sufficient to clear serious single event effects before an additional error occurs that requires ground intervention.

For single-event effects that have potential to propagate within a design, a Single Event Effect Criticality Analysis (SEECA) can be used to identify the single-event effect sensitivity and severity. Other considerations include time to detect failures, time to recover failures, system operations, and mission phases as in NASA/TM-2019-220269.

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SEE is an evolving field that encompasses a wide range of failure mechanisms and anomalous behaviors in EEEE parts. As new devices are developed and tested existing taxonomies, classifications, acronyms, and terminology are not always consistent. The project radiation engineer is best suited to identify applicable SEE requirement(s) for a given part/system/technology.

2.2 Radiation Requirements

2.2.1 Destructive SEE Requirement

RHARD-67: Destructive SEE **shall not** cause permanent failure, nor permanent degradation, of EEEE parts or systems that adversely affects spaceflight system performance or reliability.

> ***Rationale:*** *Survival of the SOLAR Observatories is dependent on individual systems tolerating the single-event effects environment. Some destructive SEEs do not cause an immediate catastrophic failure; the device may continue to function but with degraded long-term reliability, redundancy, or performance. Mitigation implemented for destructive SEE must ensure that there is no adverse effect to system performance or reliability.*

2.2.1.1 Single-Event Latchup Requirement

RHARD-72: All EEEE parts, excluding those immune by nature of their technology type, **shall** have LET_{th} for SEL greater than 37 MeV·cm^2/mg.

> ***Rationale:*** *The natural space environment has a significant reduction in particles with normally-incident LET greater than 37 MeV·cm^2/mg. This represents the minimum acceptable level for parts selection as communicated in a manner familiar to radiation engineers and system designers but does not eliminate risk entirely. 100% piece-part testing is not required; this requirement may be satisfied through board- or system-level testing at certain unique test facilities or by thorough justification of part technology, applicable past experience, modelling/simulation, or equivalent analyses. Note that higher SEL LET_{th} are desirable; parts with SEL LET_{th} greater than 75 MeVcm^2/mg may be considered immune to SEL entirely.*

2.2.1.2 Single-Event Burnout and Single-Event Gate Rupture Requirements

RHARD-77: All EEEE parts that may be susceptible to SEB or SEGR **shall** have a SEGR and SEB LET_{th} greater than 37 MeV·cm^2/mg when biased at 133% of the application's worst-case (including transient) V_{DS}, V_{CE}, V_R (or equivalent).

> ***Rationale:*** *SEB and SEGR may not be mitigable at circuit or system level without significant residual risk. The voltage applied to the part, including transient peaks, is a critical element of SEB/SEGR radiation susceptibility; in addition to LET_{th}, the voltages must be evaluated for each unique usage of a part to ensure that required derating (potentially larger than EEEE part electrical reliability derating) is met. The 133% bias*

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for test data requirement is effectively the same as derating to 75% of passing radiation test data. 100% piece-part testing is not required; this requirement may be satisfied through board- or system-level testing at certain unique test facilities or by thorough justification of part technology, applicable past experience, modelling/simulation, or other analyses.

RHARD-81: All power MOSFETs **shall** have a SEGR LET_{th} greater than 37 MeV·cm^2/mg when biased at 167% of the application V_{GS}(off) condition.

Rationale: *Power MOSFETs are susceptible to SEGR based on gate-source voltage in the off-state, particularly when over-driven into a "hard off" condition, and are particularly hard to protect at the circuit or system level. The 167% bias for test data requirements is effectively the same as derating to 60% of passing radiation test data. 100% piece-part testing is not required; this requirement may be satisfied through board- or system-level testing at certain unique test facilities or by thorough justification of part technology, applicable past experience, modelling/simulation, or other analyses.*

2.2.2 Non-Destructive SEE Requirement

RHARD-86: All systems **shall** avoid or tolerate errors due to non-destructive SEE, e.g., SEUs, SETs, SEFIs, etc.

Rationale: *Systems must avoid or tolerate non-destructive SEE to ensure the SOLAR Observatories meets performance requirements set forth in the SRD. Non-destructive SEEs are often unavoidable in EEEE parts regardless of part class, grade or heritage and are best addressed through robust system design that anticipates, mitigates, and/or tolerates anomalous behavior. A mechanism of recovery, whether autonomous or ground based, ensures continued mission operations in a SEE environment.*

RHARD-90: All EEEE parts susceptible to non-destructive SEE that perform error-vulnerable or error-critical functions **shall** be characterized in an application appropriate for the expected flight application.

Rationale: *Non-destructive SEE are often unavoidable in EEEE parts regardless of part class, grade or heritage. Other requirements impose rate calculations and system tolerance. This requirement ensures sufficient high-quality data is available to inform those two verification processes, whether by project-specific testing or collection of applicable existing data.*

RHARD-93: An analysis **shall** document heavy-ion and proton SEE performance of the system including, at a minimum, rates for all error-vulnerable and error-critical functions for each single-event effects environment described in the SRD.

Rationale: *Tolerance of non-zero SEE rates requires understanding of likelihood and criticality of the events. Rates calculated here serve to demonstrate compliance with multiple SRD performance and survival requirements of SOLAR Observatories in background, and solar flare conditions. Note that proton contribution to SEE rate may be*

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negligible for parts with LET_{th} greater than ~20 MeV·cm^2/mg and destructive SEE may be negligible for parts with LET_{th} greater than ~75 MeV·cm^2/mg.

2.2.3 TID/DDD Requirement

RHARD-98: Effects due to TID **shall not** cause permanent damage to, or unacceptable performance degradation of, spaceflight systems after exposure to the 95th percentile mission TID as specified in the SRD.

Rationale: *Establishes that TID tolerance of individual systems will be sufficient to meet project lifetime and performance requirements for the environments described in the SRD. The tabular data in the SRD establishes specific environmental parameters for the mission.*

RHARD-102: Effects due to DDD **shall** not cause permanent damage to, or unacceptable performance degradation of, spaceflight systems after exposure to the 95th percentile mission DDD as specified in the SRD.

Rationale: *Establishes that DDD tolerance will be sufficient to meet project lifetime and performance requirements for the environments described in the SRD. The tabular data in the SRD establishes specific environmental parameters for the mission.*

2.3 Spacecraft Charging

Requirements in this document do not address spacecraft and materials charging. Please see MIL-HDBK-4002B or contact project radiation engineer.

Relevant SRD Requirements:

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3 ABBREVIATIONS AND ACRONYMS

ASTM	American Society for Testing and Materials
CCB	Configuration Control Board
CM	Configuration Management
CMOS	Complementary metal–oxide–semiconductor
CO	Contracting Officer
CPARS	Contractor Performance Assessment Reporting System
CSO	Chief Safety and Mission Assurance Officer
DCMA	Defense Contract Management Agency
DDD	Displacement Damage Dose
DOC	Department of Commerce
EDAC	Error-Detection and Correction Codes
EEEE	Electrical, Electronic, Electromechanical, and Electro-optical
ELDRS	Enhanced Low Dose Rate Sensitivity
FAR	Federal Acquisition Regulations
FM	Flight Models
GFP	Government-Furnished Property
GPR	Goddard Procedural Requirements
GSFC	Goddard Space Flight Center
IT	Information Technology
JEDEC	Joint Electron Device Engineering Council
L1	Lagrange 1
LET	Linear Energy Transfer
MAR	Mission Assurance Requirements
MBU	Multiple Bit Upset
MeV	Megaelectronvolts
MIL-STD	Military Standards
MMIC	Monolithic Microwave Integrated Circuits
MOSFET	Metal-oxide-semiconductor field-effect transistor
NASA	National Aeronautics and Space Administration
NESDIS	National Environmental Satellite, Data, and Information Service
NFS	National Aeronautics and Space Administration (NASA) Federal Acquisition Regulations (FAR) Supplement
NIEL	Non-Ionizing Energy Loss
NOAA	National Oceanic and Atmospheric Administration
NWS	National Weather Service
PCP	Parts Control Plan
PPIRS	Past Performance Information Retrieval System
QA	Quality Assurance
QAP	Quality Assurance Plan
QASP	Quality Assurance Surveillance Plan
QMS	Quality Management System
RHARD	Radiation Hardness Assurance Requirements Document

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SBU	Single-Bit Upset
SEB	Single Event Burnout
SEE	Single Event Effects
SEECA	Single Event Effect Criticality Analysis
SEFI	Single Event Functional Interrupts
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SEP	Single Event Phenomena
SET	Single Event Transient
SEU	Single Event Upset
SHE	Single Hard Error
SMA	Safety and Mission Assurance
SME	Subject Matter Expert
SOLAR	Space weather Observations at Lagrange 1 to Advance Readiness
SOW	Statement of Work
SRD	Spacecraft Requirements Document
SWO	Space Weather Observations
SW Next	Space Weather Next Program
SWPC	Space Weather Prediction Center
TDMS	Technical Data Management System
TID	Total Ionizing Dose

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Radiation Effects Definitions

Displacement Damage Dose (DDD) – the mean energy deposited in a device region by radiation that goes into atomic displacements divided by the mass of the region. One common unit is MeV/g.

Linear Energy Transfer (LET) - a measure of the ionizing energy deposited per unit length as an energetic particle travels through a material. The common LET unit is MeV·cm2/mg of material.

Non-Ionizing Energy Loss (NIEL) - a measure of the energy loss per unit path length due to atomic displacements as a particle traverses a material. The common NIEL unit is MeV·cm2/g of material.

Non-recoverable Single Event Effect (SEE) – single event effects without mitigation or protection schemes (generally applies to unit/box-level and above)

Recoverable SEE – non-destructive single event effects (generally applies to unit/box-level assessments and above)

Single Event Burnout (SEB) - An event in which a single energetic-particle strike through a high electric field induces a localized high-current state in the device, resulting in catastrophic device failure or in permanent degradation that is usually characterized by a significant increase in leakage current that exceeds the manufacturer's maximum specification.

Single Event Effect (SEE) - any measurable effect to a circuit due to a single particle strike, commonly an ion or a neutron-induced secondary ion. This includes, but is not limited to, single event upsets (SEUs), single event transients (SETs), single hard errors (SHEs), single event latchups (SELs), single event functional interrupts (SEFIs), single event burnouts (SEBs), single event gate ruptures (SEGRs), and single event dielectric ruptures (SEDRs).

Single Event Functional Interrupt (SEFI) - a condition that causes loss of device functionality due to a change induced in a critical portion of a device, commonly a control structure, configuration file, or mode register. It generally requires a device reset or are initialization to resume normal device operations, but for many devices, a power cycle is necessary to initiate a full device reset to resume normal operations. A device undergoing a SEFI may simply be non-responsive or may have a sustained high-current state as it is no longer operating as designed.

Single Event Gate Rupture (SEGR) - an event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET, MOS capacitor, or floating-gate memory. An SEGR is manifested by an increase in gate leakage current and can result in either the permanent degradation or the complete failure of the device.

Single Event Latchup (SEL) - a condition that may cause device failure due to a single event induced high current state associated with the turn-on of a real or parasitic thyristor that creates a short circuit between two power supply rails. A SEL may or may not cause permanent device damage but requires power cycling of the device to resume normal device operations. In addition, SEL that appear recoverable may suffer hidden degradation and must be evaluated for latent damage (device does not fail from the immediate single particle event, but reliability is

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degraded, and premature failure may occur). Guidance on radiation test and failure analysis of SEL-induced latent damage is defined in NASA Alert NA-GSFC-2005-05.

Single Event Transient (SET) – a temporary glitch or deviation from expected operation caused by one particle, with a subsequent return to normal operating behavior.

Single Event Upset (SEU) - a change of state induced by an energetic particle such as a cosmic ray or proton in a device, such as a bit flip in memory. These are "soft" errors in that a reset or rewriting of the device will usually return the device to normal behavior thereafter.

Single Hard Error (SHE) - a SEU that causes a permanent change to the operation of a device. An example is a stuck bit in a memory device.

Single-Bit Upset (SBU) and Multiple Bit Upset (MBU) – a distinction between events that upset a single circuit node (like a memory cell) and those that upset multiple nodes (or memory cells) at once.

Threshold LET (LETth) - the maximum LET at which no SEE is observed.

Total Ionizing Dose (TID) – the mean energy deposited by ionizing radiation in a device region divided by the mass of the region. This is often given in units of rad(Si), where 1 rad(Si) = 100 erg deposited per gram of silicon.

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NASA Advisory

Goddard Space Flight Center

GSFC NASA ADVISORY

1. Advisory Number NA-GSFC-2005-05	**2. Subject** Latent Damage Reliability Issues Due to Single-Event Latchup and High-Current Error Modes.

3. Manufacturer N/A	**4. Manufacturer CAGE Code** N/A	**5. Federal Stock Code** N/A

6. Part/Material/Process Number N/A	**7. Lot Date Code/Batch Code/Serial Number** N/A	**8. Controlling Spec/Document Number** N/A

9. References

Becker et al., "Latent Damage in CMOS Devices From Single-Event Latchup," IEEE Trans. Nucl. Sci., vol. 49, no. 6, p. 3009

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11. Problem Description and Details:

When parts experience an overcurrent due to Single-Event Latchup (SEL) or other single-event effects (SEE), they may fail outright, they may suffer no damage, or they may remain functional despite having sustained "latent damage" that compromises their future reliability. This last possibility is a concern not just because of the threat it poses to part reliability, but also because it blurs the line between destructive and nondestructive SEE and because it can be very difficult and costly to determine whether a part is vulnerable to latent damage. It is important to stress that parts may sustain latent damage even if SEL detection and recovery circuitry is used. Properly addressing this threat requires both proper test procedure and proper investigation of parts after they have been tested. Finally, the facts that the study of latent damage is in its infancy and that state-of-the-art microelectronics continues to introduce new materials and device structures ensures that best practice for handling this threat will evolve rapidly. Pages 2 and 3 give additional details on contemporary best practice. However, concerned parties should consult an expert in radiation effects for the most up to date knowledge.

12. Actions Recommended:

(1) All spacecraft electronic system/subsystem designers should consult with the radiation effects engineers early in the design stage to ensure that parts potentially susceptible to SEL and latent damage are identified for testing and evaluation.

(2) Because latent damage is a relatively new threat, even "heritage" parts that exhibit "nondestructive" SEL should be evaluated for potential susceptibility.

(3) Even parts with external SEL circumvention circuitry should be evaluated for latent damage issues.

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11. Problem Description and Details: *(Continued from page 1)*

Latent Damage: Best Test and Analysis Practice for Managing Risks

Latent damage may occur any time parts experience an error mode with sufficiently high current that part reliability is compromised due to thermal stress, electromigration or other mechanisms. The most common triggering mechanism is Single-Event Latchup (SEL), although high current single-event functional interrupts (SEFIs) and other SEE modes may also give rise to currents sufficiently high to be of concern. Latent damage poses a concern not just because it may compromise device reliability, but also because it blurs the line between "destructive" and "nondestructive" SEL. The microscopic evidence of latent damage observed by Becker et al.[1] means that it is no longer sufficient that a SEL susceptible part remain functional after SEL. The prospect of latent damage also complicates other aspects of testing for potentially destructive SEE. For example, just as multiple SEL modes in a part may divide between destructive and nondestructive, some "nondestructive" modes may result in latent damage while others do not. Thus, a single dwell test, in which the part is left in a high-current SEL state for several minutes may not be sufficient to allay all latent damage concerns.

We stress that the study of latent damage is still nascent, so it is not possible to state with 100% certainty what threshold current or other characteristics an event must reach to be of concern. The study by Becker et al. found that in the parts that exhibited latent damage (Analog Devices AD9260 and National Semiconductor ADC10231 analog to digital converters and the Cardinal/Cypress CAR/CPPXIT-A7BR oscillator), the current density during SEL exceeded 1.0E7 A/cm^2. However, this study relied on visual evidence (optical microscopy or SEM) of damage (e.g. melted metallization, cracked dielectrics), and some damage may result in compromised reliability without a clear visual manifestation. Moreover, current density is not a direct observable, and must usually be calculated by dividing the peak power supply current by the minimum metallization cross section. Since test hardware may not always capture the peak current and accurate information on metal-trace cross-sectional areas may not be available, it is better to err on the side of caution. For these reasons, we place the threshold for concern at 1.0E6 A/cm^2, subject to revision as this threat is better understood.

Current Best Practice

Current best practice with regard to detection of latent damage susceptibility affects both testing and post-test procedure. With regard to testing, the main concern is that all SEL (or other SEE) modes that may be capable of causing latent damage be detected. This means that irradiating the part until one has observed SEL a few times may not be sufficient. Instead, one should irradiate parts to a predetermined fluence dictated by the acceptable failure rate and confidence level for the mission. In addition, however, one should at the very least seek to categorize the SEL modes of the part (in terms of maximum latchup current, current rise time, etc.) to determine whether different SEL modes are present and conduct a dwell test of several minutes for each SEL mode detected. Alternatively, it may be possible to detect the different SEL modes during heavy-ion testing and then conduct dwell tests using laser irradiation. In addition, several tools may be useful in characterizing various SEL modes—especially in conjunction with laser irradiation. Infrared microscopy can identify "hotspots" on the part that may indicate high thermal stress due to overcurrent conditions. In addition, Kuboyama et al.[2] have suggested use of photo-emission microscopy to detect optical photon emission that occurs due to recombination during an SEL—a means of distinguishing SEL from other high-current error modes. Such techniques may be useful not just for detecting high-current error modes but also for determining whether the high currents are carried over the entire part or are localized to a particular metal trace.

Following the above guidelines will ensure with high confidence that any vulnerability to either destructive SEL or to latent damage is realized during testing. However, one must still detect any latent damage that has occurred. The following is recommended for latent damage testing of samples after SEL testing:

1) Optical microscopy of the device (500x min, 1000x preferred)
2) Life tests with associated failure analyses
3) Thermal cycling (full-functional)
4) Maximum rating test and analysis (drive device to maximum rated limits to look for "hot spots"; use an un-irradiated device as a reference; techniques such as infrared camera or liquid crystal film might be used to detect such hot spots)
5) Repeat microscopic examination (500x min, 1000x preferred)
6) Full functionality test
7) Scanning electron microscopy (SEM)

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11. Problem Description and Details: *(Continued from page 2)*

These tests are intended to observe any latent damage that may have occurred and/or activate it so that it can be detected. Unfortunately, the process of SEE testing can itself be stressful for the parts, since even for hermetically sealed parts the package cover must be removed from the package, exposing the parts to the atmosphere and other stresses. For plastic encapsulated parts, flip-chips and other advanced packages, the stresses can be even more severe, since preparation may involve removal of the die from the package, thinning of the die and so on. In such cases, it may be difficult to determine whether the cause of any degraded performance in the life test is radiation induced or results from the pre-irradiation handling of the parts. Careful part handling, including provision of a dry nitrogen environment for parts may limit damage due to environmental factors, but this significantly increases test costs. However, to distinguish definitively between damage caused by radiation-induced overcurrent and that caused by pre-processing of the devices, it may be necessary to compare performance on the above tests for two groups of parts—the post SEL parts and a control group that has gone through the same pre-irradiation processing, but not been irradiated. Alternatives to such involved handling and testing would include:

1) Working with part manufacturers/packagers to obtain parts suitable for testing without special processing (e.g. removable lids, no metal lead frames, etc.)
2) Irradiation at an ultra-high energy heavy-ion facility like the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University where ion beams have sufficient range to penetrate device packaging.

Finally, it is essential to understand that the study of latent damage is still in its infancy and that the state of the art for dealing with this threat to microelectronic part reliability will change as the field matures. Moreover, evolution of microelectronic technology continues to introduce new materials and device structures into state-of the art microelectronics. As such consulting a radiation expert is essential if this risk is to be managed effectively.

Parts Potentially Affected

While high-current failures have been seen in bipolar technologies (e.g. Analog Devices AMP01 instrumentation amplifier), the majority of latent damage concerns arise in CMOS parts that exhibit SEL. In principle, any CMOS part that has not specifically been demonstrated to be immune to SEL (and other high-current error modes) and/or to latent damage should be considered potentially susceptible to both effects. However, of particular concern are parts fabricated on bulk CMOS—such as commercial memories (SRAM, DRAM, FLASH, ferroelectric, etc.), commercial analog-to-digital and digital-to-analog converters (especially high-precision) and so on.

References

1) Becker et al., "Latent Damage in CMOS Devices from Single-Event Latchup," IEEE Trans. Nucl. Sci., vol. 49, no. 6, p. 3009.
2) Kuboyama et al., "Pseudo and Local SELs Observed in Digital LSIs and Their Implication to SEL Test Method," accepted for the Nuclear and Space Radiation Effects Conference (NSREC) 2005.

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