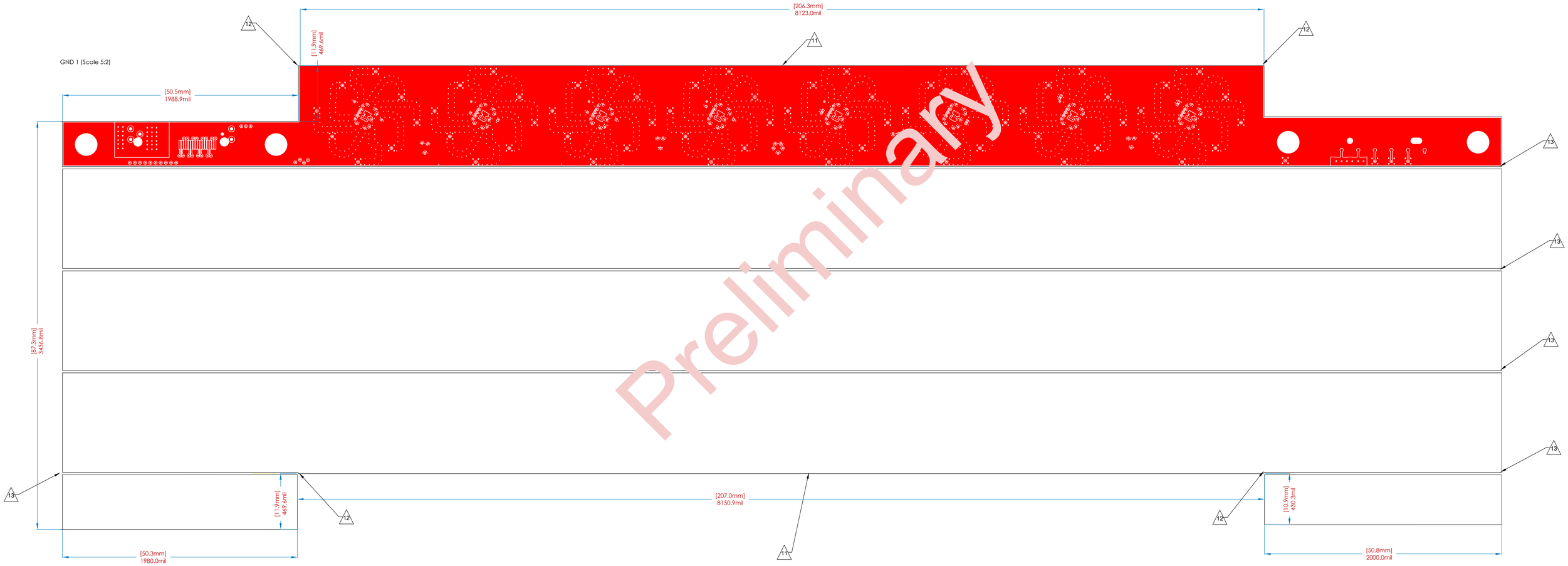
1. NO CHANGES BEYOND CUSTOMARY AND STANDARD BUILD PRACTICES SHALL BE MADE WITHOUT PRIOR APPROVAL FROM NASA GRC.
2. PRIMARY SIDE OF BOARD SHOWN ON PAGE 1 (FABRICATION DRAWING).
3. DESIGN SHALL BE IAW IPC-2221, IPC-2222, AND IPC-2226 (TYPE 4).
4. FABRICATION, INSPECTION AND ACCEPTANCE CRITERIA PER IPC-6012 CLASS 2.
5. MATERIAL:
   A. EM-892K GLASS CLOTH EPOXY LAMINATE PER IPC-4103/134. COPPER ELECTROD EPOSITED HIGH TEMPERATURE TYPE H, THICKNESS TOLERANCE CLASS B AND SURFACE QUALITY CLASS A. SEE LAMINATE STACK UP FOR NORMAL FOIL WEIGHT, UNLESS OTHERWISE INDICATED. MINIMUM DIELECTRIC SPACING BETWEEN CONDUCTIVE LAYERS SHALL BE .0025 MINIMUM AFTER LAMINATION.
   B. BONDING SHEET: EM-892K RESIN PRE-IMPREGNATED GLASS FABRIC PER IPC-4103/134.
   C. COPPER FOIL: ELECTROPLATED COPPER SHEET PER IPC-4562A, HTE-TYPE E.
      i. .25 OZ STARTING WEIGHT BEFORE PLATING FOR CONDUCTOR LAYERS WITH FINAL THICKNESS OF < .5 OZ
      ii. .5 OZ STARTING WEIGHT BEFORE PLATING FOR CONDUCTOR LAYERS WITH FINAL THICKNESS OF 1 OZ
6. CONDUCTORS: DESIGNED MINIMUM ACCEPTABLE CONDUCTOR WIDTHS AND SPACING AS FOLLOWS:
   A. INTERNAL/ EXTERNAL (INCH) CONDUCTOR WIDTH ≥ TO .013, +.003 -.003
   B. CONDUCTOR WIDTH < TO .013 AND < .025, +.004 -.004
   C. CONDUCTOR WIDTH ≥ TO .025, +.006 -.006
   D. MINIMUM SPACING OF .0040
   E. MINIMUM CONDUCTOR WIDTH OF .005
7. IMPEDANCE TO BE MAINTAINED PER TRANSMISSION LINE TABLE ON PAGE 1 OF THIS DRAWING.
8. MINIMUM ANNULAR SOLDER RING SHALL BE: .001 EXTERNAL AND .001 INTERNAL OF COPPER PAD ANNULAR RING, NOT INCLUDING HOLE PLATING MATERIAL, AROUND DRILL HOLES FOR ELECTRICAL CIRCUITS.
9. SOLDER MASK:
   A. APPLY A SINGLE COAT OF LPI (LIQUID PHOTO IMAGEABLE) PERMANENT BLUE SOLDER MASK ON PRIMARY (TOP) AND SECONDARY (BOTTOM) SIDE BOARD OVER BARE COPPER PER IPC-SM-840 CLASS T. FOR SOLDER MASK USE ARTWORK MASTER SUPPLIED.
10. FINAL FINISH:
   A. EXPOSED COPPER AREAS SHALL BE PLATED WITH GOLD
      i. GOLD PLATING TO BE ENIG (Electroless Nickel/Immersion Gold)
11. CHAMFER MARKED EDGES AT 45 DEGREES. CHAMFER TO START ON TOP LAYER WITH THE REMOVAL OF 62MILS OF MATERIAL AND TAPER TO 8MILS AT THE BOTTOM LAYER. COPPER WILL BE EXPOSED IN THE PROCESS AND CONNECTED WITH EDGE PLATING AS INDICATED IN NOTE 11.
12. EDGE PLATE REQUIRED WITHIN INDICATED REGION. PLATING TO CONNECT TO NET 'GND'. PLATING TO BE 1 MIL.
13. PERFORM CONTROLLED DEPTH ROUTING FROM LAYER 1 'GND 1' ALONG LINE INDICATED BY THIS NOTE. TOOL PATH DEFINED BY MECHANICAL LAYER 'ROUTE TOOL PATH'. ROUTING TO LEAVE BETWEEN 10 – 15 MILS OF DIELECTRIC MATERIAL ABOVE LAYER 7 'SL (RF 2)'.
14. SILKSCREEN, LEGENDS AND OTHER NOMENCLATURE ON TOP OF THE SOLDER MASK USING WHITE EPOXY INK PER MFG INSTRUCTIONS. FOR SILKSCREEN USE ARTWORK MASTER SUPPLIED. MANUFACTURER TO CLIP SILKSCREEN THAT INTERFERES WITH SOLDER/PASTE MASKS.MANUFACTURER TO INDICATE THE FOLLOWING:
   A. MANUFACTURER ID
   B. DATE CODE
   C. SERIAL NUMBER: STARTING AT 001 INCREMENT SERIAL NUMBER FOR EACH PCB MADE
15. PRINTED WIRING BOARD AND TEST COUPON TO BE DESIGNED TO THE REQUIREMENTS OF IPC-2221 CLASS 2 AND TESTED PER IPC-6018 CLASS 2 TYPE 4.
   A. ELECTRICAL TEST SHALL BE PERFORMED ON 100% OF THE DELIVERABLE PRODUCT. THE ELECTRICAL PROGRAM SHALL BE EXTRACTED FROM GERBER DATA OR IPC-356 FILE.
   B. FOREIGN INCLUSIONS ALLOWED: 2 PER SIDE OF BOARD.
   C. LAYER TO LAYER MIS-REGISTRATION ALLOWED: MAX .003. TOTAL OF .006 OVER ALL LAYERS.
   D. TOTAL MASS LOSS (TML) OUTGASSING TEST NOT REQUIRED.
   E. DIELECTRIC WITHSTANDING VOLTAGE LAYER TO LAYER: PER IPC-6018. TO BE DONE ON TEST COUPON.
   F. RATING: MAXIMUM RATED VOLTAGE: 28VDC. TESTING TO BE AT DOUBLE THE MAXIMUM RATED VOLTAGE.
16. TEST COUPONS TO BE INTEGRATED INTO PANEL PER IPC-2221 CLASS 2 ARE TO BE ADDED BY MFG.
   A. TEST COUPONS TO BE TRACEABLE TO LOT AND PWB SERIAL NUMBER.
   B. TEST COUPON TO BE LOCATED WITHIN .5 INCHES OF ANY BOARD ON THE PANEL.

Transmission Line Structure Table

Impedance Id	Transmission Line	Target Impedance	Calculated Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Gap	Reference layers	Substack	Clearance	Target Tolerance
1	Coated Microstrip	50	50.04	GND 1	10.00mil(0.25mm)	10.00mil(0.25mm)		RF1	Board Layer Stack	5.00mil(0.13mm)	20%
2	Edge-Coupled Coated Microstrip	100	119.12	GND 1	5.00mil(0.13mm)	5.00mil(0.13mm)	11.00mil(0.28mm)	RF1	Board Layer Stack	5.00mil(0.13mm)	10%
3	Offset Stripline	50	41.65	RF1	8.00mil(0.20mm)	8.00mil(0.20mm)		GND 1,GND 2	Board Layer Stack	5.00mil(0.13mm)	20%
4	Edge-Coupled Offset Stripline	100	100.01	RF1	4.80mil(0.12mm)	4.80mil(0.12mm)	5.00mil(0.13mm)	GND 1,GND 2	Board Layer Stack	5.00mil(0.13mm)	10%
5	Offset Stripline	50	62.76	GND 2	5.00mil(0.13mm)	5.00mil(0.13mm)		RF1,Power	Board Layer Stack	5.00mil(0.13mm)	20%
6	Edge-Coupled Offset Stripline	100	100.00	GND 2	5.81mil(0.15mm)	5.81mil(0.15mm)	5.00mil(0.13mm)	RF1,Power	Board Layer Stack	5.00mil(0.13mm)	10%
7	Offset Stripline	50	59.09	Control	5.70mil(0.14mm)	5.70mil(0.14mm)		RF1,Power	Board Layer Stack	5.00mil(0.13mm)	20%
8	Edge-Coupled Offset Stripline	100	100.00	Control	5.81mil(0.15mm)	5.81mil(0.15mm)	5.00mil(0.13mm)	RF1,Power	Board Layer Stack	5.00mil(0.13mm)	10%
9	Offset Stripline	50	54.06	Power	5.00mil(0.13mm)	5.00mil(0.13mm)		Control,GND 3	Board Layer Stack	5.00mil(0.13mm)	20%
10	Edge-Coupled Offset Stripline	100	100.01	Power	4.80mil(0.12mm)	4.80mil(0.12mm)	5.00mil(0.13mm)	Control,GND 3	Board Layer Stack	5.00mil(0.13mm)	10%
11	Offset Stripline	50	49.98	GND 3	9.26mil(0.24mm)	9.26mil(0.24mm)		Power,SL (RF 2)	Board Layer Stack	5.00mil(0.13mm)	20%
12	Edge-Coupled Offset Stripline	100	99.99	GND 3	6.10mil(0.16mm)	6.10mil(0.16mm)	5.00mil(0.13mm)	Power,SL (RF 2)	Board Layer Stack	5.00mil(0.13mm)	10%
13	Offset Stripline	50	50.72	SL (RF 2)	9.00mil(0.23mm)	9.00mil(0.23mm)		GND 3,FEED (GND 4)	Board Layer Stack	5.00mil(0.13mm)	20%
14	Edge-Coupled Offset Stripline	100	100.27	SL (RF 2)	6.00mil(0.15mm)	6.00mil(0.15mm)	5.00mil(0.13mm)	GND 3,FEED (GND 4)	Board Layer Stack	5.00mil(0.13mm)	10%
15	Surface Microstrip	50	49.99	FEED (GND 4)	87.72mil(2.23mm)	87.72mil(2.23mm)		Power	Board Layer Stack	5.00mil(0.13mm)	20%
16	Edge-Coupled Surface Microstrip	100	100.01	FEED (GND 4)	19.64mil(0.50mm)	19.64mil(0.50mm)	5.00mil(0.13mm)	Power	Board Layer Stack	5.00mil(0.13mm)	10%

GND 1 (Scale 5:2)



Preliminary

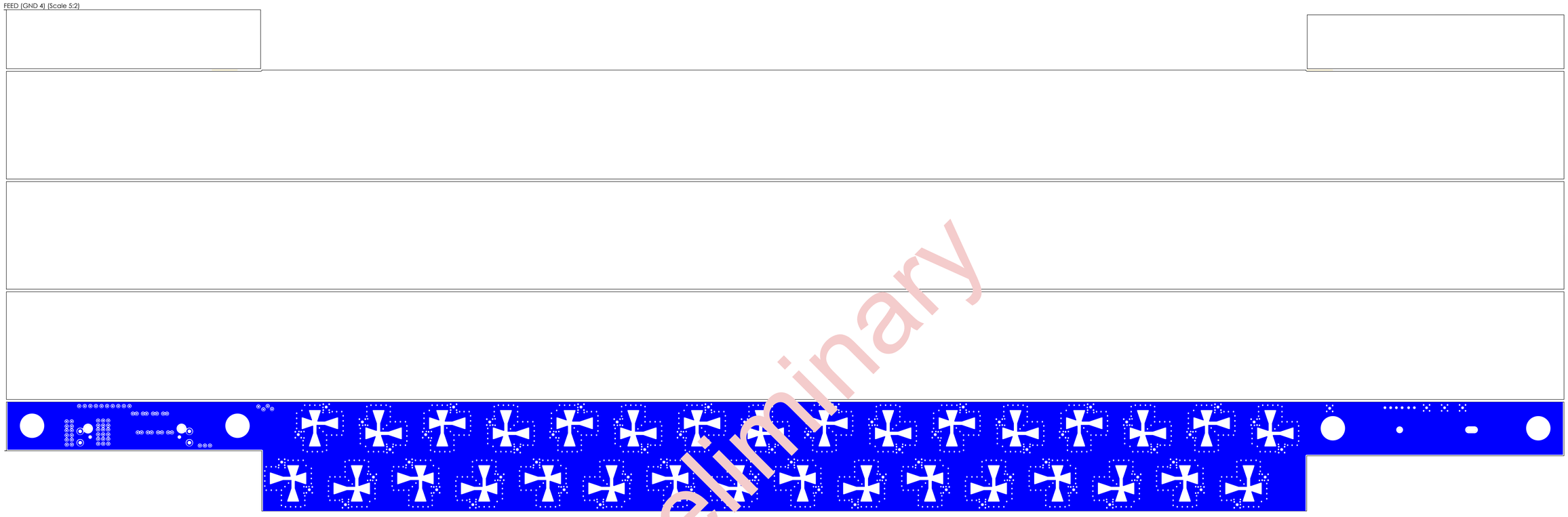
APPROVALS	DATE
ENGINEER:	
DESIGNER:	
CHECKER:	
Reference Documents	
BOM DOC:	
FAB DOC:	
SCH DOC:	
PCBA DOC:	

PART NO: =PCB_PART_NUMBER

NASA Glenn Research Center
21000 Brookpark Rd
Cleveland, OH 44135

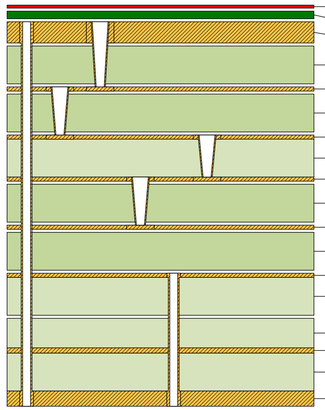
DESIGN ITEM: .Item
DESIGN ITEM REVISION: .ItemRevision
TITLE: =PCB_FABRICATION_DRAWING_TITLE
SIZE: D
DWG NO:
REV:
SCALE: =Scale
FILE NAME: ADaPT GEN III PCB, Fabrication
SHEET: 1 OF 4

FEED (GND 4) (Scale 5:2)



Preliminary

Layer Stack Legend

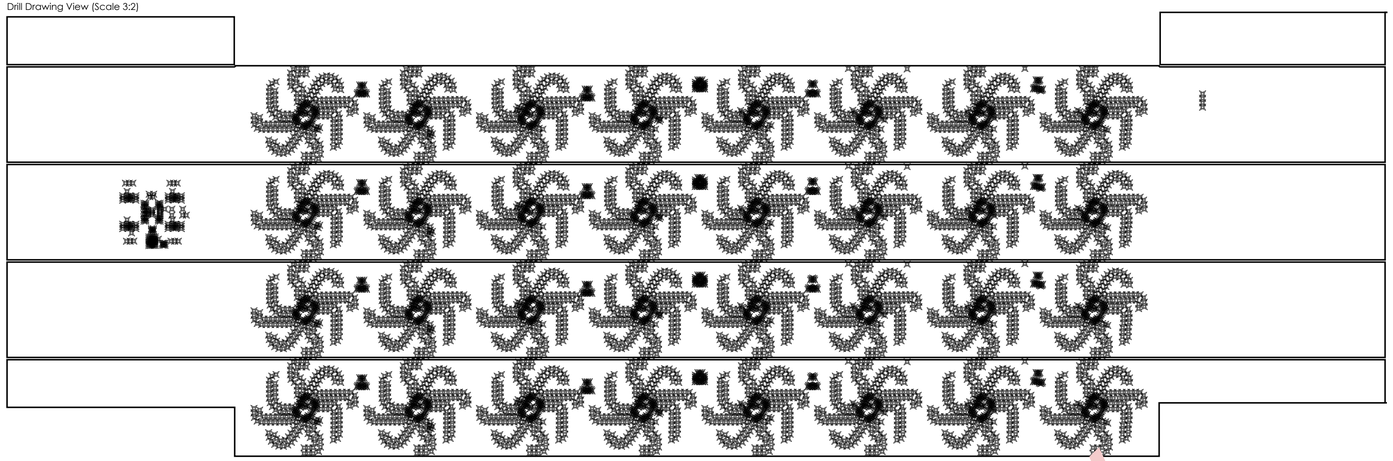


Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	1.00mil	Solder Resist	Solder Mask	GTS
Copper	**GND 1**	**2.80mil**		**Signal**	**GTL**
Prepreg		*5.00mil*	*EM-892K*	*Dielectric*	
Copper	**RF1**	**0.55mil**		**Signal**	**G1**
Prepreg		*5.00mil*	*EM-892K*	*Dielectric*	
Copper	**GND 2**	**0.55mil**		**Signal**	**G2**
Core		*5.00mil*	*EM-892K*	*Dielectric*	
Copper	**Control**	**0.55mil**		**Signal**	**G3**
Prepreg		*5.00mil*	*EM-892K*	*Dielectric*	
Copper	**Power**	**0.55mil**		**Signal**	**G4**
Prepreg		*5.00mil*	*EM-892K*	*Dielectric*	
Copper	**GND 3**	**0.55mil**		**Signal**	**G5**
Core		*20.00mil*	*TSM-DS3b*	*Dielectric*	
Core		*3.90mil*	*Composite dielectric*	*Dielectric*	
Copper	**SL (RF 2)**	**0.70mil**		**Signal**	**G6**
Core		*5.00mil*	*TSM-DS3b*	*Dielectric*	
Copper	**FEED (GND 4)**	**2.01mil**		**Signal**	**GBL**

Total thickness: 63.16mil

SIZE	DWG NO:	REV:
D	=PCB_FABRICATION_DRAWING_TITLE	
SCALE: 3:2	FILE NAME: ADAPT GEN III PCB, Fabrication	SHEET: 2 OF 4

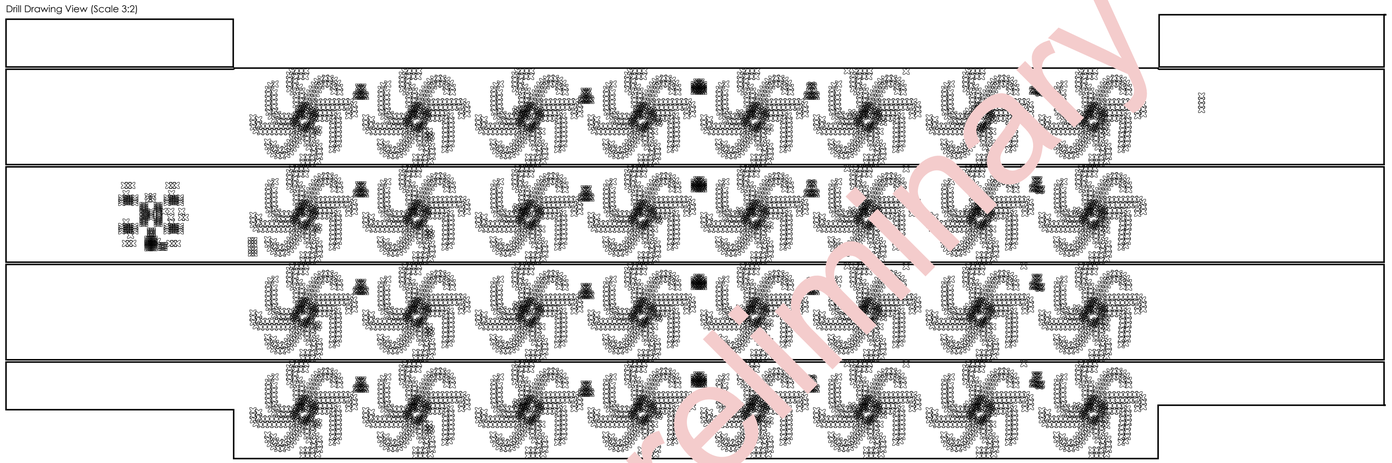
Drill Drawing View (Scale 3:2)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Hole Tolerance
⌘	8334	7.00mil(0.18mm)	Plated	[UVIA] GND 1 - RF1	+/-2.00mil(0.05mm)
	8334 Total				

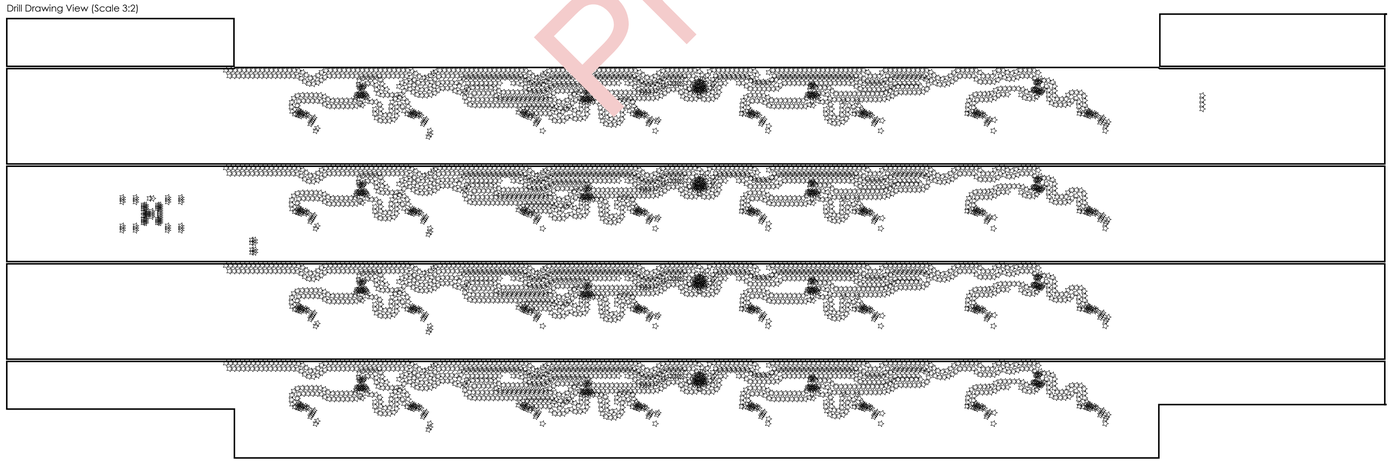
Drill Drawing View (Scale 3:2)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Hole Tolerance
⌘	8078	7.00mil(0.18mm)	Plated	[UVIA] RF1 - GND 2	+/-2.00mil(0.05mm)
	8078 Total				

Drill Drawing View (Scale 3:2)

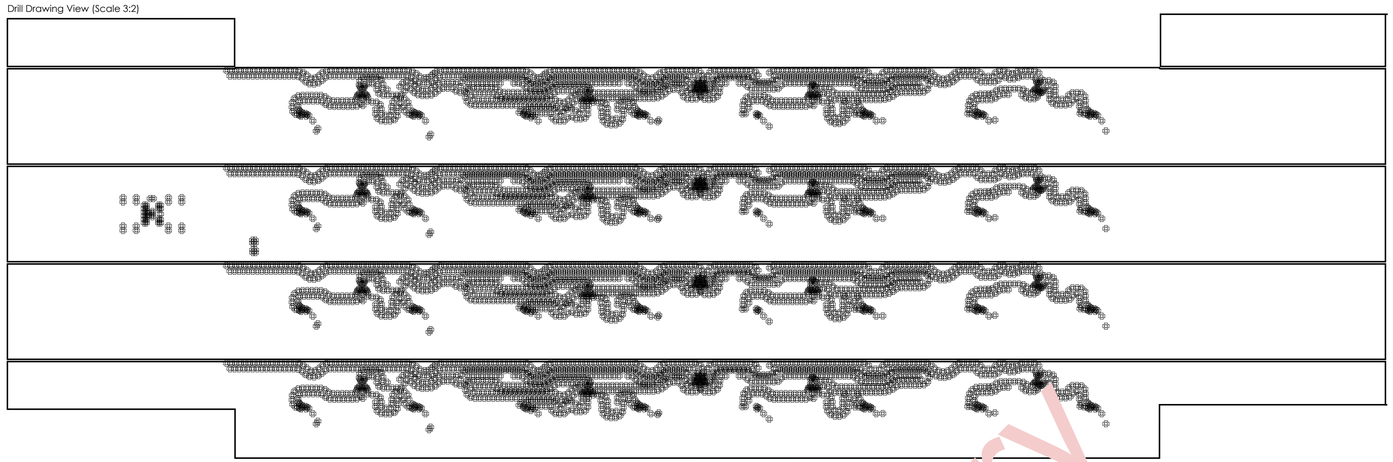


Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Hole Tolerance
☆	5623	7.00mil(0.18mm)	Plated	[UVIA] GND 2 - Control	(Mixed)
	5623 Total				

Preliminary

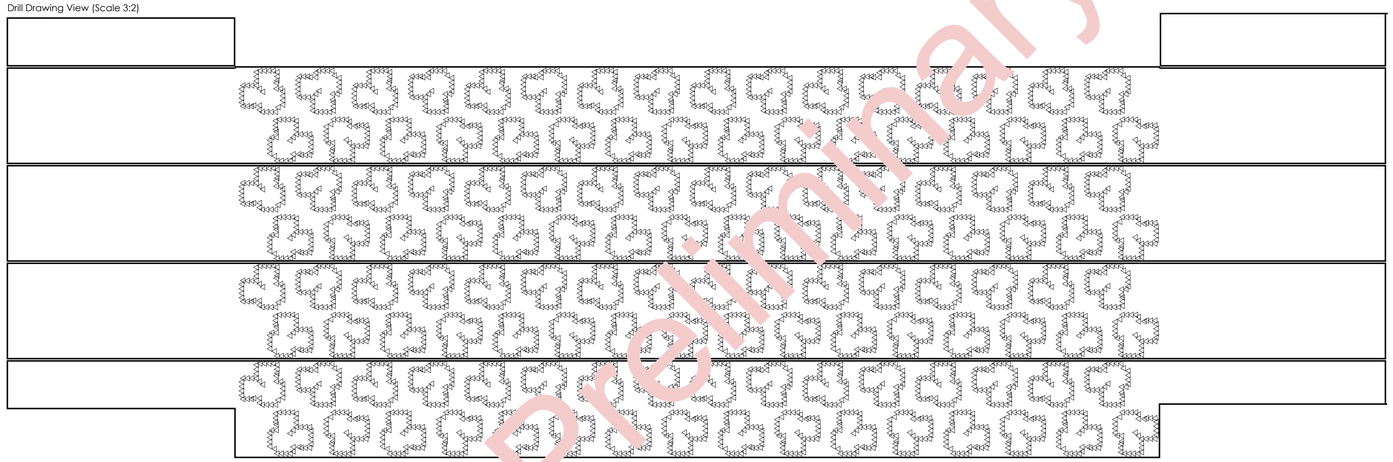
Drill Drawing View (Scale 3:2)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Hole Tolerance
⊕	5338	7.00mil(0.18mm)	Plated	[UVIA] Control - Power	(Mixed)
	5338 Total				

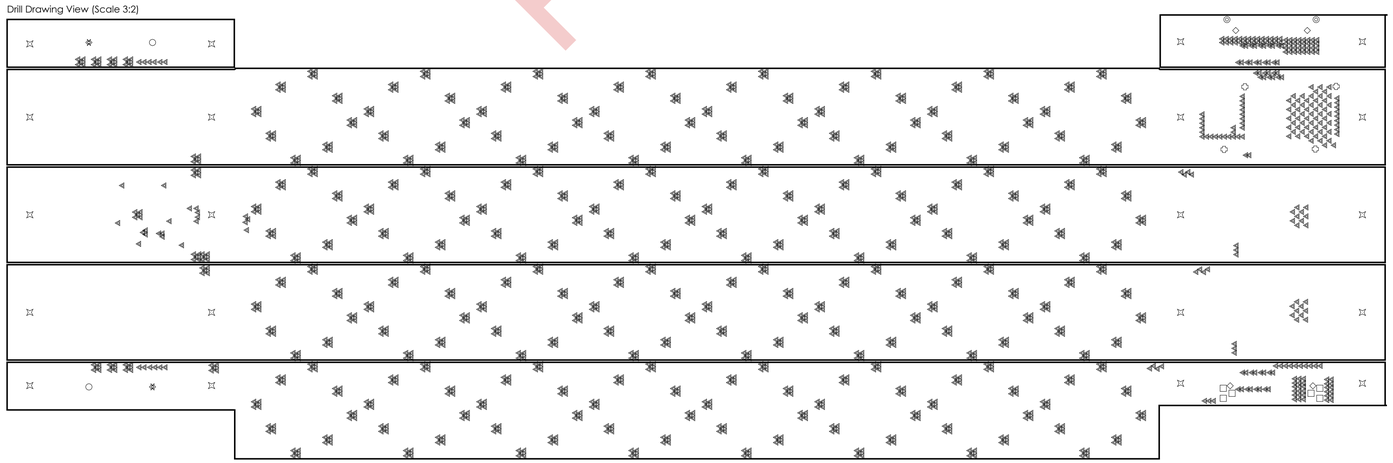
Drill Drawing View (Scale 3:2)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Hole Tolerance
☆	5623	7.00mil(0.18mm)	Plated	[UVIA] GND 2 - Control	(Mixed)
	5623 Total				

Drill Drawing View (Scale 3:2)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Hole Tolerance
▼	1668	12.00mil(0.30mm)	Plated	GND 1 - FEED (GND 4)	+/-3.00mil(0.08mm)
□	6	27.56mil(0.70mm)	Plated	GND 1 - FEED (GND 4)	
✲	2	33.00mil(0.84mm)	Non-Plated	GND 1 - FEED (GND 4)	
○	2	34.00mil(0.86mm)	Non-Plated	GND 1 - FEED (GND 4)	
◎	2	45.28mil(1.15mm)	Plated	GND 1 - FEED (GND 4)	+/-1.97mil(0.05mm)
◌	4	47.24mil(1.20mm)	Non-Plated	GND 1 - FEED (GND 4)	
◇	4	57.09mil(1.45mm)	Non-Plated	GND 1 - FEED (GND 4)	(Mixed)
⌘	20	170.00mil(4.32mm)	Non-Plated	GND 1 - FEED (GND 4)	+/-1.97mil(0.05mm)
	1708 Total				

Preliminary